WHAT IS CLAIMED IS:

1. A method comprising:

restoring a future file over more than one clock cycle when a termination occurs.

2. The method of Claim 1, further comprising maintaining the future file in a pipelined processor,

3. The method of Claim 1, wherein restoring the future file comprises updating at least some speculative registers in the future file with architectural values.

4. The method of Claim 1, wherein more than one clock cycle comprises two clock cycles.

5. The method of Claim 1, wherein more than one clock cycle comprises three clock cycles.

6. The method of Claim 1, wherein more than one clock cycle comprises the number of clock cycles it takes to flush the pipelined processor.

7. An apparatus comprising:

a control unit coupled to a first set of registers, a second set of registers and a pipeline, the control unit adapted

to restore the first set of registers with data contained in the second set of registers over more than one clock cycle following a termination of an instruction in the pipeline.

8. The apparatus of Claim 7, wherein each register in the second set of registers is associated respectively with a register in the first set of registers.

9. The apparatus of Claim 7, wherein more than one clock cycle comprises two clock cycles.

10. The apparatus of Claim 7, wherein more than one clock cycle comprises three clock cycles.

11. The apparatus of Claim 7, wherein the control unit is further adapted to flush the pipeline following the termination of the instruction in the pipeline.

12. The apparatus of Claim 11, wherein more than one clock cycle comprises the number of clock cycles it takes to flush the pipeline.

13. The apparatus of Claim 12, the control unit further adapted to restore at least one register in the first set of registers after the pipeline has been flushed.

14. The apparatus of Claim 7 wherein the pipeline is an X-stage pipeline, the control unit adapted to restore the first set of registers with data contained in the second set of registers over X-N clock cycles or fewer, following a termination of an instruction in an N^{th} stage of the pipeline.

15. A system comprising:

a static random access memory device;

a processor coupled to the static random access memory device, wherein the processor includes a first set of registers, a second set of registers, a pipeline and a control unit adapted to restore at least some of the registers in the first set of registers with values in at least some of the registers in the second set of registers over more than one clock cycle if a termination occurs in the pipeline.

16. The system of Claim 15, wherein more than one clock cycle comprises two clock cycles.

17. The system of Claim 15, wherein more than one clock cycle comprises three clock cycles.

18. The system of Claim 15, wherein the control unit is further adapted to flush the pipeline following the termination of the instruction in the pipeline.

19. The system of Claim 18, wherein more than one clock cycle comprises the number of clock cycles it takes to flush the pipeline.

20. The system of Claim 19, the control unit further adapted to restore at least one register in the first set of registers after the pipeline has been flushed.

21. The system of Claim 15, wherein the pipeline is an X-stage pipeline, and wherein the control unit is adapted to restore the first set of registers with data contained in the second set of registers over X-N clock cycles or fewer, following a termination of an instruction in an N^{th} stage of the pipeline.